Towards Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs and TFETs

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The III-V vertical nanowire (VNW) MOSFETs is one of the candidates under consideration for CMOS technology beyond the 7 nm node [1]. This device architecture brings together the superior transport properties of III-V semiconductors [2] with the ultimate scalability of a vertical nanowire channel [3] where gate length, spacer thickness and contact length do not contribute to the footprint of the device [4]. With a similar geometry, III-V VNW TFETs potentially allow lower voltage operation and extreme high energy efficiency [5]. This is due to the TFET ability to achieve a subthreshold swing (S) below 60 mV/dec at room temperature (RT), a physical limit to MOSFETs [5]. III-V vertical nanowire MOSFETs and TFETs have been demonstrated by bottom-up [6-8] and top-down approaches [9-11]. Future ultra-scaled logic applications demand VNW FETs with sub-10 nm diameter [4]. Achieving this, remains an elusive goal. The difficulty lies in creating VNWs with a small diameter and a high aspect ratio, in contacting such thin VNWs, and altogether in addressing the integration challenges posed by such deeply scaled transistor structures. To our best knowledge, to date, the narrowest VNW transistor that has been claimed is an InAs/GaSb TFET with a diameter of 11 nm, but no electrical characteristics were shown [8]. In the Si system, 18 nm diameter VNW MOSFETs has been demonstrated [12].

At MIT in the last few years, we have focused on demonstrating and exploring the physics of sub-10 nm diameter III-V MOSFETs and TFETs. We have adopted a top-down approach for VNW formation based on precision reactive ion etching [13]. RIE enables nanowires with a diameter of 20 nm and an aspect ratio >10. Further diameter scaling can be obtained through digital etch (DE) [13]. This consists of an oxidation step in O_2 plasma and an oxide removal step in a diluted acid. By separating both steps, the process is self-limiting and yields a very precise etching rate. In this way, we have been able to reduce the diameter of InGaAs VNW to ~12 nm. We have also shown that DE improves the sidewall electrical characteristics. Further diameter scaling using water-based acid DE becomes impossible. Below a diameter of ~12 nm, the nanowires collapse due to the strong mechanical forces during oxide removal and the subsequent rinsing and drying steps of the DE process. We have recently solved this problem by using alcohol-based acids with a much lower surface tension [14]. Using the same oxidation step, the new technique shows a radial etch rate of 1 nm/cycle, identical to the conventional water-based approach. Sub-10 nm diameter nanowires with a high yield and mechanical stability have been achieved. In particular, InGaAs nanowires with diameter of 5 nm and an aspect ratio > 40 have been demonstrated, as shown in Fig. 1 [14].

Another challenge to obtain functional sub-10 nm VNW transistors is contacting the tiny NW top. The use of non-alloyed contact metals such as Mo has been found to result in what appears to be a non-conducting peripheral region that we have termed the “dead zone” [15]. This imposes a scaling limit to the contact diameter below which the electrical connection opens up. By introducing a thermal annealing step, we have been able to shrink the VNW diameter that yields working ohmic contacts to 15 nm [16].

Our recent research efforts have resulted in the demonstration of the first 15 nm diameter VNW InGaAs MOSFETs. Fig. 2 shows the output, transfer and subthreshold characteristics of a typical device [16]. This is a single-nanowire transistor. Its extremely small scale explains the “noisy” characteristics. Remarkably, an outstanding linear subthreshold swing of 69 mV/dec is obtained indicating excellent interfacial quality of the VNW sidewall. Further scaling to sub-10 nm diameter requires understanding and addressing the origin of the “deadzone” associated with the top ohmic contact.

An interesting aspect of the physics of such small devices is their seemingly “noisy” electrical characteristics. With such a small size, charging and discharging of a single trap center results in significant and very visible changes in the I-V characteristics, as can be seen in Fig. 2. We are in the process of studying this phenomenon. In preliminary measurements of single-VNW TFETs with D=40 nm, we have observed prominent Random Telegraph

Noise with a characteristic $1/f^2$ frequency spectrum (Fig. 3). These studies should shed light on the role of traps and defects in the operation of ultra-scaled VNW FETs and the implications for future CMOS technologies.

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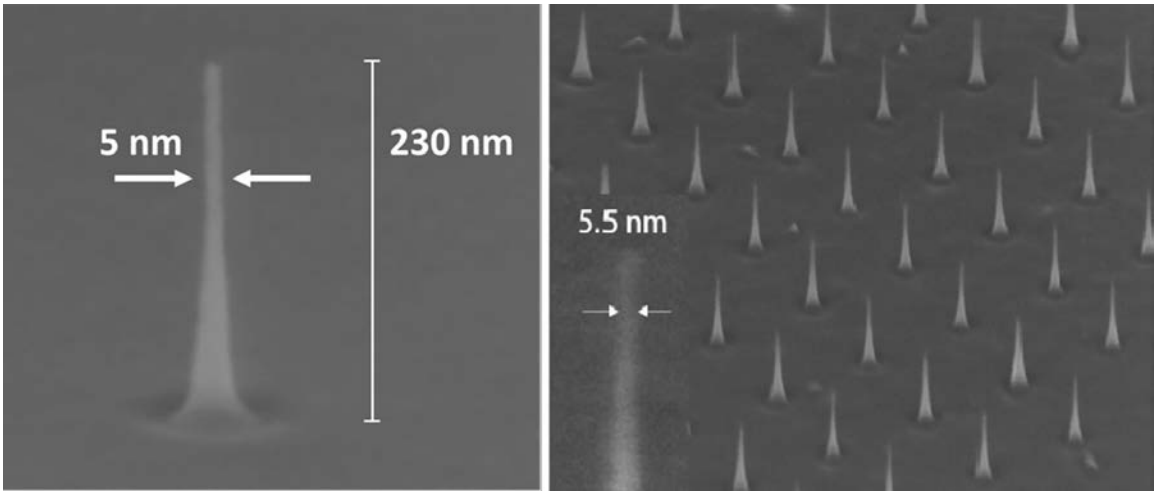

Figure 1. Left: InGaAs VNW with 5 nm diameter, 230 nm height obtained after 10 cycles of digital etch in 10% H_2SO_4:methanol. Right: D=5.5 nm InGaAs VNW array after 7 DE cycles in 10% H_2SO_4:methanol. The yield is 90%.

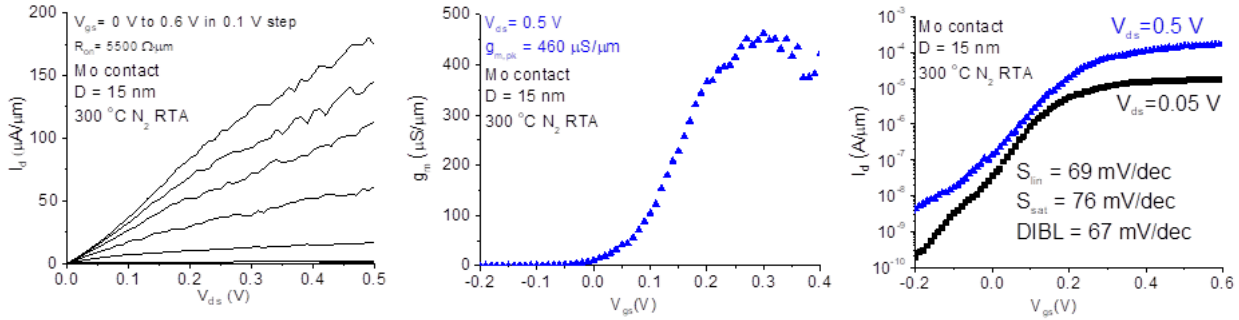

Figure 2. From left to right, output, transconductance and subthreshold characteristics of an exemplar D = 15 nm InGaAs single VNW MOSFET with Mo contact metal after 300ºC FGA for 1 min.

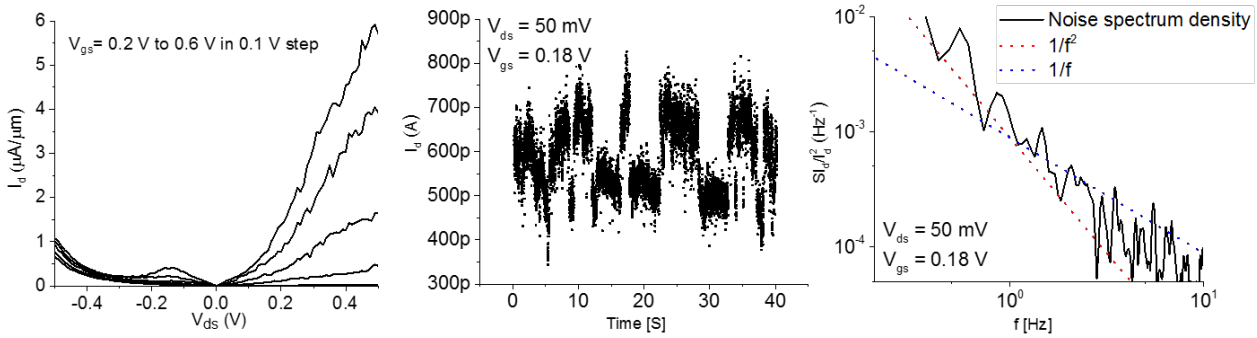

Figure 3. Left: Output characteristics of D=40 nm InGaAs TFET showing the $V_{ds}<0$ regime where a clear Esaki negative differential resistance region is evident. Center: Drain current at the indicated bias of the same device. Clear Random Telegraph Noise (RTN) is visible. Right: Frequency spectrum of signal on center figure. A distinct $1/f^2$ regime characteristic of RTN is observed.